Evaluation of a 4 K 4-Stage Pulse Tube Cryocooler for Superconducting Electronics

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ABSTRACT

Market applications of digital and mixed-signal superconducting electronics require the integration of a robust, long life, highly efficient 4 K cryocooler with an equally robust cryopackage including superconducting integrated circuits (ICs). The ideal 4 K cryocooler, with full reliability, power and cost efficiency, and manufacturability, is not yet commercially available. Recently, a custom-designed laboratory prototype of a 4 K 4-stage Stirling-type pulse-tube cryocooler was produced by Lockheed-Martin and delivered to HYPRES. We have adapted the system with a cryopackage which we used to mount and successfully test a superconducting IC with a variety of Nb circuits including an RSFQ binary counter. For 600 W total compressor power and a package with broadband input-output lines, extended stable operation of the counter at T=4.5 K was demonstrated with a clock frequency up to 46 GHz clock speed, with 25 mW of excess cooling capacity on the coldest stage (4.5 K). The thermodynamic and mechanical performance is promising for the development of an improved compact cryocooler for superconducting electronic applications such as wireless communications.

INTRODUCTION

The deployment of high performance superconducting electronics in many application platforms requires the integration of a robust, long life, highly efficient 4K cryocooler with an equally robust cryopackage including superconducting integrated circuits (ICs). In the 1980's and 1990's the main electronics application pursued was in the field of electronic instrumentation, including sampling oscilloscopes and primary voltage standard systems.[1,2,3] While such applications remain an option for a limited size market, an exciting new potential emerged since the year 2000, targeting the field of wireless communications. Using superconducting electronics, and specifically ICs comprised of many Josephson junctions exhibiting ultrafast rapid-single-flux-quantum (RSFQ) logic, the potential exists for developing and deploying radio transceivers that can revolutionize wireless communication systems. The improvements include the realization of true "Software Radio"[4] which requires full digital processing at multi-GHz radio frequencies, and is achievable only with RSFQ superconducting electronics. Such a software radio transceiver system can result in universal interoperability among all protocols, compatibility with legacy systems, the most efficient use of the wireless spectrum, overall savings in capital as well as operating expenditures, "future-proofing" by enabling pure software upgrades of the systems, and, for military systems, the highest level

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of encryption and security. Along with this promise comes the stringent requirement for the indispensable cryocooler: besides efficiency and ruggedness, maintenance-free operation for over five years is a necessary requirement.

The superconducting electronics community has continually sought the ideal cryocooler for its applications. The focus in the present paper is on cryocoolers for niobium-based ICs, since only this superconductor has demonstrated the scalability and yield needed for an IC process. This requires operation at or near the boiling point of liquid helium (<5 K), which inevitably implies a multistage cryocooler. In contrast, there has been a developing market for passive analog radio-frequency (RF) filters based on high-temperature superconductors (HTS) that can operate at temperatures of 60 K or above. Cryocoolers for HTS devices are typically single-stage and fairly compact and efficient, with considerable progress in recent years in performance and reliability for commercial applications.

Multistage cryocoolers for low-temperature superconductor (LTS) electronic applications are still developing toward full commercial viability. The past two decades have witnessed steady progress in the availability of cryocoolers adequate for the industry's applications. When HYPRES introduced its 70-GHz sampling oscilloscope in 1987,[1,2] no cryocooler met its requirements and the product was introduced based on an open cycle liquid-helium cooling system. In the 1990's when HYPRES introduced its cryocooled primary voltage standard system[3], the first units were based on the HS-4 3-stage cryocooler (2-stage G-M + J-T), requiring 2 separate compressors for its operation as well as water cooling for the compressors. Later, Leybold introduced a 2-stage G-M cryocooler (the now discontinued 4.2LAB system with ~2 kW single-phase power and air cooled) using rare earth regenerators and this system was adopted for the next generation metrology systems. The most helpful advance occurred at the beginning of the new century (~ year 2000) with the introduction of the 0.1 W Sumitomo 2-stage G-M system [Model RDK-101D], which in the US operates at ~ 1.2 kW (air cooled) and comfortably exceeds its specification of 0.1 W at 4.2K. This cryocooler is now used by HYPRES as the "workhorse" of all its product offerings in instrumentation, as well as the platform for all prototype receiver and transceiver systems demonstrating the potential of this application.[5]

While progress has been very encouraging, the cryocooler offerings fall short of what is required to enable the electronics applications to take hold.[6] Although the benefits of cryocooled superconducting electronic systems are established and accepted, the "cryophobia" displayed by the potential customers continues to get in the way of the true blossoming of this huge market. At the heart of the requirement is the need for a "turnkey" maintenance-free cryocooler which can be ruggedized for deployment onto fixed as well as moving platforms while also having sufficient efficiency to justify any increased system cost.

During the past 5 years, HYPRES has been researching the options available for such a cryocooler, and working with US Government experts to identify a candidate for an initial prototype. Within the resources available to support such a development, a single program was started in 2005 with Lockheed Martin Advanced Technology Center as the cryocooler developer to produce a laboratory prototype of a 4-stage Stirling-type pulse tube cryocooler compatible with the goals described above. This prototype was delivered to HYPRES at the end of 2007 and was described by Lockheed Martin (LM) at the 2007 CEC-ICMC conference.[7] Since its delivery, we have reproduced the thermal evaluation of the LM cryocooler, fitted it with a cryopackage accommodating a sample superconducting IC, and evaluated the performance of the circuit within the cryocooler. Further, we have determined the next steps required to evolve such a design into a field prototype, as well as the requirements of other cryocooler solutions which will be welcome if/when available from other cryocooler developers. We report in this paper on these findings and results.

THE CRYOCOOLER

A multistage pulse tube system was selected as being the mostly likely to offer long-term reliability (5 years or more) and ruggedness in a commercial design; there are no moving parts at low temperatures to wear out. The relatively high operating frequency (on the order of tens of Hz) of the Stirling-type pulse-tube is also advantageous as compared with a low-frequency GM-type pulse tube, in that it reduces the low-temperature thermal oscillations and vibrations that can be

difficult to damp out. A multistage cooler also offers the potential of mounting auxiliary components, such as HTS filters and cooled low-noise semiconductor amplifiers, on the other stages.[8]

The 4-stage pulse tube cryocooler[7] developed by Lockheed-Martin has cooling available at nominal temperatures of 70 K, 30 K, 9 K and 4.5 K, and has 2 separate compressors and working gases: ^{4}He for the top two stages and ^{3}He for the bottom (colder) two stages. While ^{3}He is often regarded as an exotic, expensive gas, its reduced boiling temperature (3.2 K instead of 4.2 K) implies ideal-gas-type performance down to lower temperatures, enabling higher heat lift at the lowest temperatures.[9] Further, in the Lockheed-Martin design, the ^{3}He compressor operates at a much lower pressure than the ^{4}He compressor, so that the total cost of the ^{3}He gas should not be prohibitive, even for a practical commercial system.

Figure 1 shows the cryostat with the water-cooled dual opposed compressor mounted on the ISO-400 vacuum top plate, through which all the necessary electrical feedthroughs penetrate. For simplicity and ease of use of the prototype, the vacuum can shown is considerably oversized (by at least 100% in volume) from the point of view of the cold-head and electronic packaging, but is simply matched to the top plate. Figure 1 also shows the cryocooler attached to its tilt-stand which enabled us to install additional cold components to a conveniently inverted cryocooler. The compressors are powered by analog power amplifiers and monitored by power meters; their pistons' positions are continuously monitored and are protected against over-stroke by an interlock system. In general, the piston strokes are balanced to keep vibrations to a minimum.

THERMAL TESTING AT HYPRES

After the unit was shipped from Lockheed-Martin, we performed an initial set of tests to verify refrigeration capacities. Table 1 shows that indeed the pulse tube achieved the same, if not better, performance as that measured by Lockheed in their Palo Alto facility under steady-state conditions with input power of 680 W. Figure 2 shows that the 4th stage refrigeration is a relatively weak function of compressor input power, which suggests there would be a wide range of compressor powers that could be used to provide the necessary refrigeration, whilst maintaining the niobium superconducting circuitry at the required temperature of 4.5 K.

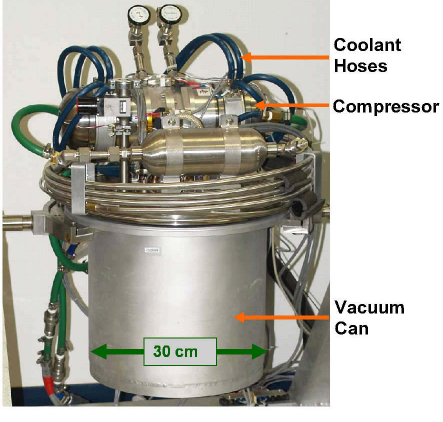

Figure 1. Complete pulse tube cryostat for superconducting electronics laboratory demonstration

Table 1. Thermal tests showed agreement of the measurements at LM and at HYPRES

	T1st (K)	Q1st (W)	T2nd (K)	Q2nd (mW)	T3rd (K)	Q3rd (mW)	T4th (K)	Q4th (mW)
LM July '07	66.7	4.3	27.4	0	9.88	0	4.5	40.7
HYPRES Nov.'-07	65.74	4.23	26.6	0	9.43	0	4.5	43.3

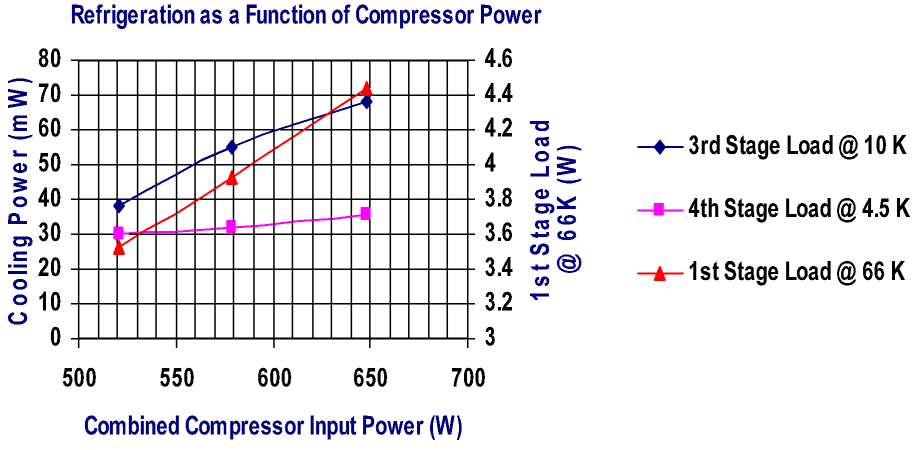

Figure 2. Refrigeration at 3 stages as a function of combined compressor input power

Interplay between the 2nd, 3rd and 4th stages

Prediction of the ability of the cryocooler to sustain the multistage heat-loads from a superconducting electronics cryopackage requires knowledge of the interplay between simultaneous heat-loads on the different stages. For the complex Rapid Single Flux Quantum (RSFQ) ICs [10,11] that are targeted for this pulse tube, the on-chip dissipation of heat at 4.5 K is relatively small (a few mW) compared to the loads from both bias-current wiring and high speed input/output wiring.[12] Heat from the wiring must be intercepted as efficiently as possible by the upper 3 stages, so the influence of loading at the warmer stages on the available refrigeration at 4.5 K is important to understand. We chose to measure the performance under conditions of regulated 1st and 4th-stage temperature with floating 2nd at 3rd stages. For Nb superconducting electronics the 4th stage would be regulated at 4.5 K (maximum operating temperature of the circuitry) and the 1st stage would be regulated at 69 K to prevent suboptimum performance caused by pressure collapse.

Figure 3 shows that cooling on the 3rd stage is mostly available at the expense of 4th stage cooling (up to about 30 mW on the 3rd stage does not affect the 4th). On the other hand, about 150 mW can be applied to the 2nd stage without affecting the fourth (with no heat applied to the 3rd stage).

THE CRYOPACKAGE

As one of the goals of this project, a 5 mm-square chip was designed and fabricated at HYPRES, with the intent of comparing its operation in liquid helium and when mounted on the 4th stage of the pulse tube cryocooler. The chip contains typical circuit elements that form part of the communications chips referred to earlier and is shown in Figure 4. Specifically, the binary counter is an RSFQ circuit that forms the core of digital decimation filters and other fast digital processing elements. This is designed to operate at digital clock speeds in excess of 40 GHz. The other circuit elements include standard RSFQ signal conditioning elements that convert between sub-mV, picosecond pulses and more standard voltage-level signals for conventional electronic processing.

The term cryopackage applies to all the apparatus necessary to support the operation of the chip apart from the cryocooler itself. This includes mechanical support, provision of the correct thermal environment, all input/output leads and all magnetic shielding required to provide sub-milliGauss magnetic fields. In general, leads are required for circuit biasing as well as high-speed analog and digital inputs, outputs, and control and monitoring circuitry. The chip is conduction-cooled to 4.5 K and mounted inside 2 nested cylindrical shields; the combined set of parts constitutes the IC module, which is shown in Figure 5.

Wiring used to span the temperature differences from 4.5 K to room temperature consisted of twisted pairs of single-conductor brass wire for the dc bias currents and low-speed signals, and stainless steel UT-47 coaxial cables for the high-speed signals. All 48 of the dc wires were ther-

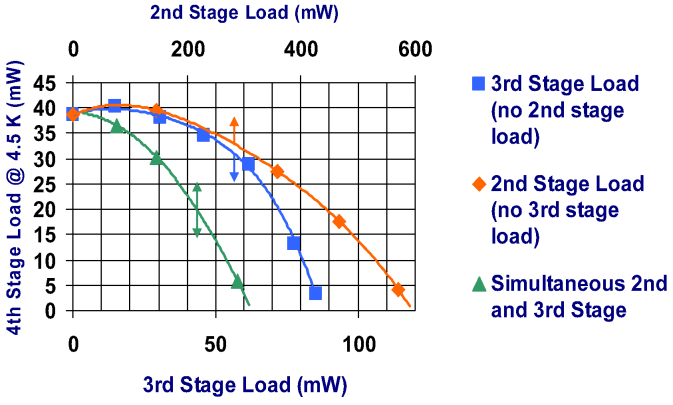

Figure 3. Fourth stage refrigeration power available at 4.5 K as a function of 2nd and 3rd stage heat loads, where the 2nd and 3rd stage loads are applied separately and simultaneously at a fixed ratio of 5:1. The input power to the compressor is 680 W and ~ 5 W is simultaneously applied to the first stage.

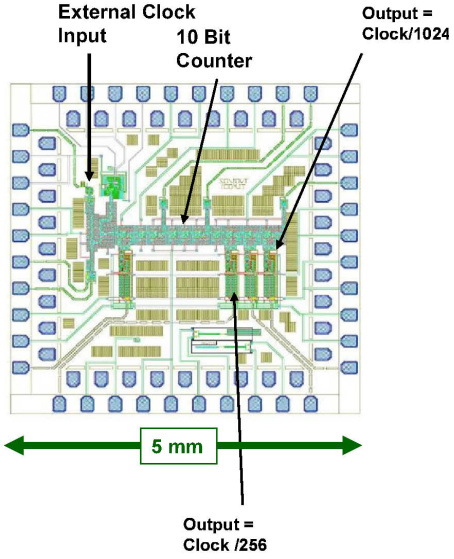

Figure 4. Layout of 5 mm superconducting test chip featuring key circuit elements of RSFQ digital receiver chips

mally sunk to all 4 stages, but for convenience the coaxial lines were not attached to the 3rd stage. The biasing lines were not optimized for minimum heat leaks,[12] but length and thickness of the wires spanning the stages were chosen for practicality; their calculated heat-loads are shown in Table 2.

Using the experimental results shown in Figure 3 and the calculated heat-loads from above, we predicted the available refrigeration at 4.5 K for the unbiased chip condition. The measured loads were either read directly from changes in heater power within a control loop or by shifts in temperature of a given stage. Discrepancies are apparent on the 1st and 4th stages; the excess heat load on the 1st stage is believed to be caused by holes in the multilayer insulation (MLI) from wiring penetrations; the excess heat to the 4th stage could be caused by imperfect thermal anchoring and/or room temperature radiation shining through to the fourth stage. Overall, the loading of the cryocooler from the cryopackage is close to what we would expect, and there was 28 mW of excess capacity at 4.5 K in the unbiased condition.

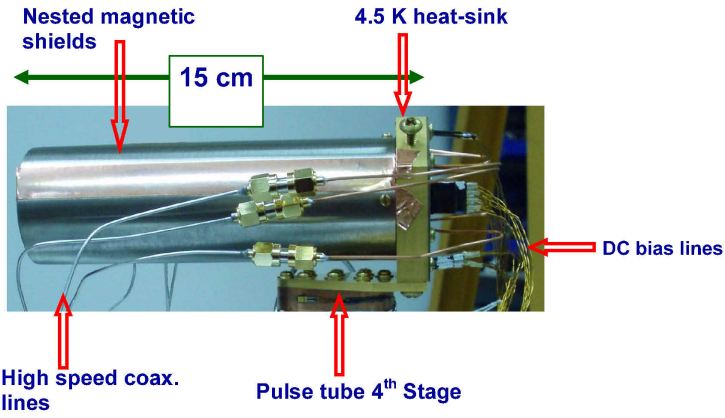

Figure 5. 4 K part of the cryopackage: the RSFQ IC module including ì-metal magnetic shields which are about 14 cm in length.

Table 2. Parameters of the leads linking the RSFQ circuits to the room-temperature connectors.

	UT-47 Stainless Steel Coaxial Lines (6 off)		30 AWG Brass Wires (48 off)		TOTAL	
Stage Temp.	Wire length between Stages (m)	Heat Load per Stage (mW)	Wire Length between Stages(m)	Heat Load (no current) (mW)	Calculated Load (mW)	Measured Load (mW)
300 K						
	0.1		0.15			
70 K		175		330	505	900
	0.06		0.16			
30 K		24		26	50	50
			0.07			
9 K	0.08			16	16	17
			0.07			
4.5 K		3		2	5	8-10

CIRCUIT TEST RESULTS

The key test circuit in this chip is the high frequency counter. This circuit enables a high frequency signal applied from an external clock to be decimated down by a known factor (2^N where N is the number of the counter stage) and to produce a lower frequency output which can be readily measured. The ratio between this measured output and the high frequency input then allows the determination of successful operation of the chip. The counter used here had 10 bits and so the ratio between input and output is 2^{10} or 1024. For example, an external clock signal of up to 40 GHz would appear at the 10^{th} bit output decimated down to 39 MHz and this circuit operation was verified in liquid helium. Besides correct operation, the output signal – usually a very low level ~100 ìV signal from the RSFQ circuit – was also successfully amplified by the on-chip amplifier to a level greater than 2 mV for frequencies in the 10-200 MHz range.

The chip was then mounted on the cryocooler and the tests repeated. Successful operation of the counter was again obtained with an external clock frequency up to 46 GHz, as shown in Figure 6. The dc bias margin for operation was in excess of +/-10% at clock frequencies exceeding 20 GHz, a very encouraging result as far as circuit stability.

FUTURE DEVELOPMENT

The program discussed in this paper successfully produced a laboratory prototype of a cryocooler based on technology that has been space qualified in other cryocooler implementations. Furthermore, it demonstrated the successful integration and operation of superconducting circuit. The next top-level milestone is the demonstration of a "field" prototype, i.e., an integrated cryocooler which can be demonstrated on an actual wireless communication system platform. Such a platform can be either the ground station of a satellite communication system, a Navy ship, a ground vehicle, or one of many other deployment platforms – military or commercial. To reach this goal through a follow-on to this program, a number of specific improvements have been identified:

- Improved efficiency of both the cold head and compressor through iteration of the designs based on the detailed measurements and feedback from this laboratory prototype.
- Ruggedization and packaging in an air-cooled enclosure. The ruggedization standards vary depending on platforms, the most forgiving of which are the ground based fixed installations. The size of the enclosure also depends on the platform, but a general guide is a size of 50x56x56 cm^3 for ground and shipborne installations and 50x24x46 cm^3 for vehicular deployments.
- Development and interfacing of compact drive electronics for both the cryocooler and the superconducting circuits. These electronics drivers must also conform to the same ruggedization standard and fit within the same enclosure.

Alternative approaches to realizing the desired crycooler can also be considered and would be welcome. The general requirements, in addition to the size envelope indicated above, ruggedness and 5 year maintenance-free lifetime, are:

- Multistage (at least 2, 3 or more are preferred for improved cryopackaging efficiency) with the lowest stage lower than or equal to 4.5K and the highest stage lower than or equal to 75K.
- Heat lifts of 50 mW (threshold) to 100 mW (objective) at (or below) 4.5 K and 5 W or more at (or below) 75K.
- Total electrical input power (wall power) for operation as well as environmental heat management of below 1 kW (800 W or lower desired).
- Total weight at or below 25 kg.

SUMMARY

We have evaluated a 4-stage Stirling-type pulse tube cryocooler developed by Lockheed Martin (LM) and providing over 40 mW at 4.5K at the lowest stage. The thermal performance reproduces the results obtained by LM and presented at the 2007 CEC-ICMC.[7] As a laboratory prototype we have also integrated, within this cryocooler, a cryopackage containing a superconducting circuit

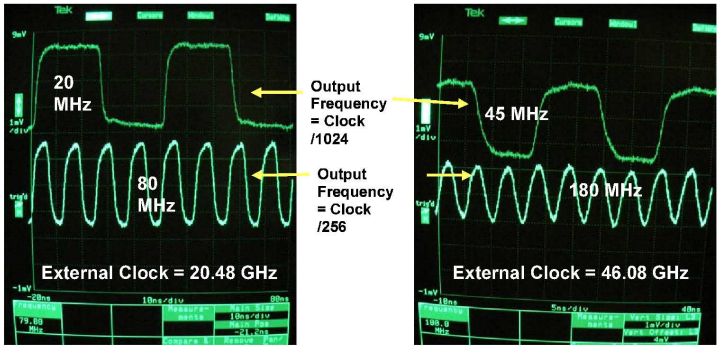

Figure 6. Output signals from counter circuit mounted on the cryocooler with 20.5 GHz and 46 GHz clock input.

and demonstrated circuit operation above 46 GHz. Identified improvements and packaging can evolve this design into a field prototype for demonstrating high performance transceivers for wireless communications. The key steps for this evolution have been identified and can equally apply to alternative approaches for other cryocooling systems.

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