# Integrated Testing of the Iris LCCE and NGAS Micro Pulse Tube Cooler

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## ABSTRACT

The Northrop Grumman micro pulse tube (micro) is a long-life (>10 years), extremely compact and lightweight (<800 g) cryocooler with the capability of supporting a wide range of applications. Previously published experimental results demonstrated cooling between 50K and 150K with over 1.2 W of cooling capacity at 80K with a rejection temperature of 300K. The strong legacy of the micro pulse tube which has a Technology Readiness Level (TRL) of 9 makes this cooler attractive for critical, risk-averse missions. The Iris Low Cost Cryocooler Electronics (LCCE) has been designed to provide basic cryocooler electronics functionality in a radiation hardened, space-compliant physical package. Much of the complexity of traditional space cryocooler electronics, such as fine multi-harmonic active vibration cancellation, has been eliminated in the interest of reducing cost, size, and mass. The targeted mass and volume design requirements for the spaceflight version of LCCE are 700 g and less than 35 cubic inches, respectively. This compact size and low mass makes the LCCE well suited for the NGAS micro pulse tube cooler. Integrated testing of the micro and a brass-board version of the LCCE has been performed. Automated cool down, temperature stability, and high efficiency DC-AC power conversion have all been demonstrated. Test results are presented, and the integrated testing of the micro pulse tube and a brass-board version of the LCCE has been performed. Test results are presented, and the path forward to a space-qualified version is discussed.

## INTRODUCTION

Space cryocooler systems, which are used for cooling infrared sensors for surveillance, weather, and deep space astronomy applications, consist of two major subsystems, the thermodynamic mechanical unit (TMU) and the cryocooler control electronics (CCE). It is a generally accepted truism among the space infrared user community that CCE technology lags TMU technology with respect to Technology Readiness Level (TRL) and Manufacturing Readiness Level (MRL) almost without exception. This poses a continual acquisition challenge in that the CCE tends to drive risk, cost, and schedule for most programs. In some cases an otherwise optimal TMU technology is rejected because a mating CCE of sufficiently high TRL and MRL does not exist.

Although the TMU portion of cryocooler systems has traditionally received the greatest attention, the design of the CCE is far from routine. Designing spaceflight rated, high reliability, radiation hardened electronics introduces huge challenges in parts selection and availability, both in

*Cryocoolers 17,* edited by S.D. Miller and R.G. Ross, Jr.

terms of the passive and active components. Functionality easily implemented using commercial components, such as low voltage power supplies, current sensing, and surge limiting, must be implemented using more basic building blocks. The limited number of available discrete values for inductors, capacitors, and, to a lesser extent, resistors also complicates the design. Long lead time parts together with minimum buys for space grade components puts additional design and programmatic constraints on the development. This is the reason why the industry has found that for spaceflight cryocooler systems, it is often the electronics that drives the schedule and the cost, not the TMU.

To avoid the cost for extensive nonrecurring engineering (NRE) associated with the development of a new CCE "from scratch" for every new cryocooler and infrared payload, Iris Technology is developing cryocooler electronics products that are applicable for a wide range of cryocooler vendors and cryocooler types. The first of these products was the Modular Advanced Cryocooler Electronics (MACE), which to date has been developed to the brass-board level and has been used to successfully drive two different Raytheon hybrid cryocoolers. The results from the first of the two integrated cryocooler-MACE tests have been published[1]. This paper describes the testing of a simplified version of MACE called the Low Cost Cryocooler Electronics (LCCE). Whereas MACE addresses the need for high input power (>500 W), multistage cryogenic refrigeration, LCCE supports nominally 100 W input power class cryocoolers, typically providing up to a few watts of cooling around 70 K. The LCCE use case is typical for a very wide range of space applications, and this is an operational regime that can be supported with a wide range of low cost space cryocoolers and/or long life tactical coolers, for which an example of each is cited here[2,3].

Although the focus of the LCCE development effort and the subject testing to date has been with an eye towards spaceborne applications, it should be noted that LCCE does have applicability to tactical applications. Production tactical military hardware programs typically desire multiple sources for key components, such as cryocoolers. LCCE provides an option by which a single CCE can support multiple tactical coolers so that a failed cooler TMU does not necessitate the replacement of the CCE, even if a different vendor's TMU technology is used. Furthermore, the legacy of LCCE to the high reliability demands of space will greatly benefit present programs on which the existing CCE being supplanted is often a low reliability component.

In the paragraphs to follow, recent testing of a low cost, commercial brass-board of the LCCE with the Northrop Grumman micro Pulse Tube Cooler (uPTC) is described. These test results support our thesis that a single, properly architected CCE design can be employed to support a wide range of cryocoolers. The data presentation is preceded by a brief discussion of the LCCE Program and the product development plan to put the following technical discussion in context.

## TECHNICAL BACKGROUND

LCCE is unique from any other cryocooler electronics available by providing a fully space-qualified, radiation hard (>300 krad total ionizing dose, TID) solution at an affordable price. Components have been selected for high reliability; per MIL HDBK 217, the calculated reliability for the LCCE is > 0.985 for 7 years of operation, which is over 550 years mean time before failure (MTBF). Since LCCE has been architected from the bottom up with the eventual recurring cost as a priority, the expected cost of the LCCE in small lot production is a fraction of the cost of "traditional" space cryocooler electronics. This has been accomplished primarily through designing out complexity that is not required for many cost sensitive missions (e.g., Operationally Responsive Space), and in so doing achieving a tremendous reduction in the radiation-hard parts cost and software development. Specifically, the LCCE provides just the basic functionality required to drive and control the cryocoolers of interest, such as dual motor drives, temperature control, and a customizable command interface. Advanced functionalities which tend to drive the cost, such as input current ripple attenuation and exported vibration mitigation, are not part of the basic design; they are provided with auxiliary electronics in the applications where they are required. The unit tested for the present effort is the basic LCCE without these additional functions.

As of this writing, the spaceborne LCCE design is complete and the space-level parts are on order. The flight-design LCCE, shown in Figure 1, is projected to enter Qualification Testing in October, 2012. The version tested, shown in Figure 2, is functionally identical for the purposes of

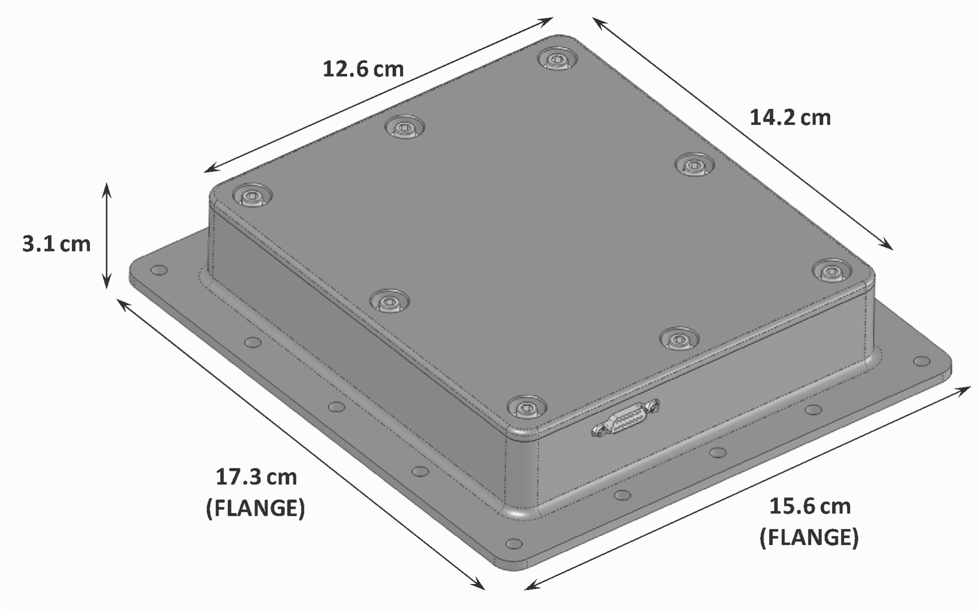


**Figure 1**. Solid model of the spaceflight version of the Low Cost Cryocooler Electronics (LCCE). Preliminary mass estimate is 700 g.

these experiments. This unit was constructed using commercial off the shelf (COTS) electronic components to provide an inexpensive test bed for risk reduction experiments and design verification. These experiments, the results of which are described herein, were to demonstrate that a single set of cryocooler electronics could be made to work well with a variety of cryocoolers to prove the basic premise of the underlying development effort. The COTS LCCE was also the test bed for the firmware development, of which an estimated 90% (based upon lines of VHDL code) will port directly over to the spaceflight LCCE.

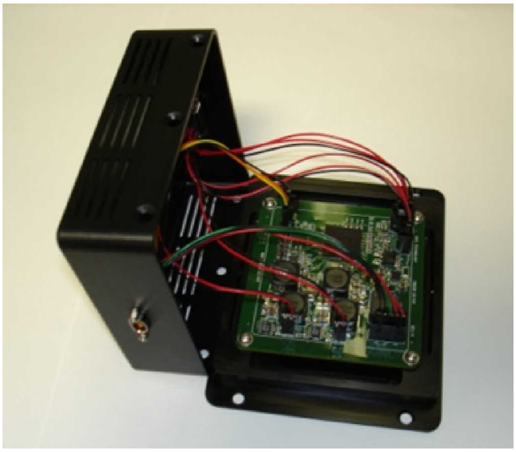

**Figure 2.** Photograph of the COTS LCCE used for this testing. The primary differences between this and the spaceflight version are the use of commercial electronic parts and the laboratory-level physical housing, which relies upon convection cooling and does not protect against harsh structural loads.

## LCCE TECHNICAL DESCRIPTION

### Spaceflight LCCE

A block diagram of the spaceflight LCCE hardware is shown in Figure 3. The core function of the LCCE hardware is fulfilled by four separate half-bridge drivers, which allow the electronics to be configured to drive a 100W two phase motor, two separate two phase motors of up to 50W each, or a single 3-phase motor of up to 75W. The drives are fronted by a surge protector that protects the hardware in case of a motor fault or damaging radiation induced transient in the motor drives. Two temperature sensor input channels accept either resistance temperature detector (RTD) or diode type sensors. The channels can be configured as primary or redundant, or the redundant channel can be wired to a compressor housing or some other temperature of interest for reporting back to a higher level controller. Control is handled entirely in an anti-fuse based FPGA, with variable control parameters passed through an RS422 interface and stored in a 128kB external radiation hardened EEPROM.

The firmware located in the FPGA has the primary function of controlling the temperature to the requested set point by modulating the amplitude of the motor drive signal. The motor drive configuration, frequency, loop tuning, and other reconfigurable parameters are loaded from the EEPROM, which allows limited reconfigurability of the hardware after the onetime programmable anti-fuse FPGA is loaded. The block diagram is provided in Figure 4.

### Differences between COTS and Spaceflight Versions

As previously indicated, the primary purpose of the COTS LCCE was to verify that a single electronics design could be made to work conveniently with a wide range of cryocoolers. For the test to have meaning, the COTS LCCE must evidently maintain fidelity relative to the intended

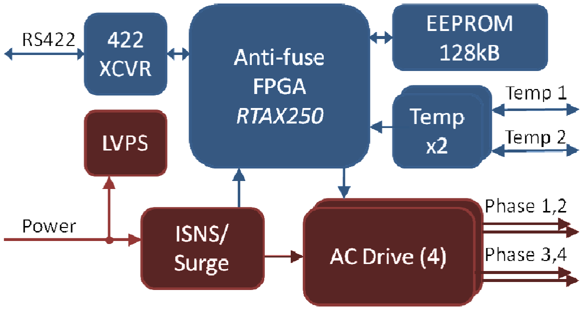


**Figure 3.** LCCE block diagram. XCVR = transceiver. LVPS = low voltage power supply. ISNS = current sense. Temp = temperature.

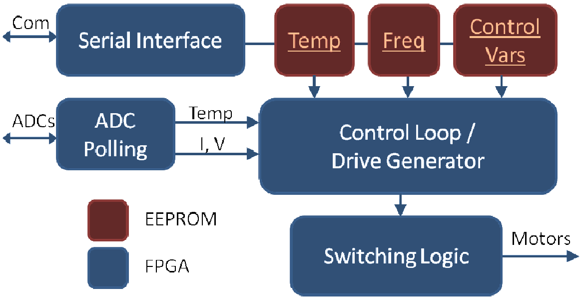


**Figure 4.** LCCE firmware block diagram. Freq = the drive frequency of the mating cryocooler. Vars = user-selectable variables.

spaceflight design, particularly with respect to the key drive and control functions. This was achieved, but there were some differences worth noting.

The controller selection for spaceflight is severely limited by the total ionizing dose (TID) and single event upset (SEU) requirements of 300 krad (Si) and SEU latch up immunity (LET) >75 MeV/mg/cm$^2$. Even with the assumption that the components need only be qualified to 100 krad (Si) and that the aluminum housing will provide the required additional shielding, this still greatly complicates the flight design. The eventual design decision was to use a onetime programmable ("single shot") anti-fuse FPGA with the addition of an external EEPROM to allow for the needed reconfigurability. The COTS FPGA uses a Xilinx SRAM-based part with integrated nonvolatile memory. This is a much more convenient format for code development and experimentation. Most of the VHDL-based control logic is portable directly between devices, with minor additional work to modify the code to use the Actel primitives.

The low voltage power supplies in the prototype COTS LCCE consist of off-the-shelf switching and linear regulators. The spaceflight version on the other hand uses a custom designed single-ended primary-inductor converter (SEPIC) to reduce size and make up for the lack of readily available and inexpensive COTS converters. The input surge limiter is a function in the flight design that is completely missing from the prototype board. It was judged necessary for protection in the case of a motor or electrical fault for an actual flight program but not necessary for laboratory experimentation.

### Test Setup Overview

Laboratory cooler testing was performed with the COTS version of the LCCE hardware, powered by a 24V external power supply to simulate the spacecraft power bus and a PC in lieu of a payload computer. Control and data links were provided via serial connection from the PC. A custom software interface as depicted in Figure 5 was created to provide a convenient means by which to control the coolers, including setting the proportionality and integral constants for the PI temperature control loop, and to facilitate data acquisition. The crycocooler controlled is seen in Figure 6.

Temperature data were collected through the primary (control) diode LCCE telemetry and a secondary calibrated cold-tip diode through a Lakeshore diode controller. Efficiency measurements were obtained using two channels of an AC power meter, one for the input side of the electronics and one for the output side of the electronics.

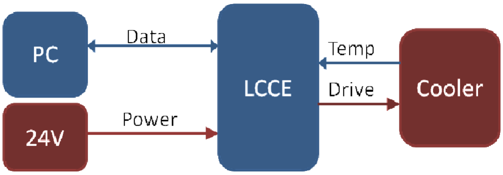


**Figure 5.** COTS LCCE test setup.

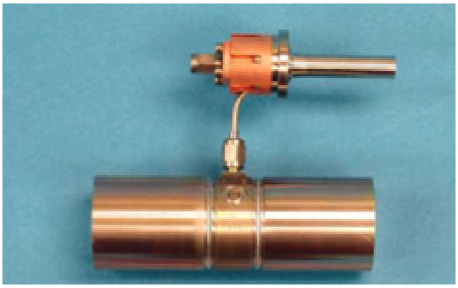

**Figure 6.** Northrop Grumman (NG) Micro Pulse Tube Cooler (µPTC), a long-life, extremely compact (<1 kg) cryocooler for low cost, long life space missions[5]

## TEST RESULTS

### Overview

The NG Micro PTC ( uPTC) test results shown were collected at the Northrop Grumman Space Park Cryocooler Laboratory in Redondo Beach, California by Tanh Nguyen et al. Previously reported data for the NG Micro PTC were obtained running the Iris LCCE open loop – these data show sub 100mK stability closed loop temperature regulation on the uPTC with the default control parameters.

### NGC uPTC Test Data

Figure 7 shows the performance of the LCCE/uPTC in terms of cold tip temperature and consumed input power versus time with transient thermal load and setpoint. The uPTC was driven to 100K with no load, then a step 1.0W thermal load was applied to the cold tip. After stabilization, the setpoint was adjusted to 76K and the temperature was allowed to settle again. Figure 7 shows the data collected under these conditions with automatic temperature enabled:

Figure 8 and 9 shows temperature stability results for the 100K, 1W and 76K, 1W conditions, respectively.

### LCCE Efficiency w/ NG Micro PTC

The constant overhead "tare" power of the LCCE was measured to be 550mW. The cable loss was calculated based upon wire gauge and length to be 150mW at the peak output power to the cooler (~40W). These losses are not accounted for in the efficiency graph of the DC-to-AC motor drives, which was fairly constant between 91% and 92% at the 40-50W load level for the uPTC. The results are shown in Figure 10.

## CONCLUSION

A COTS version of the LCCE was used to successfully drive and perform automatic temperature control with the NGC uPTC. This testing was accomplished with no modification to the LCCE hardware and firmware, and was performed at NG with a supplied LCCE unit and control interface.

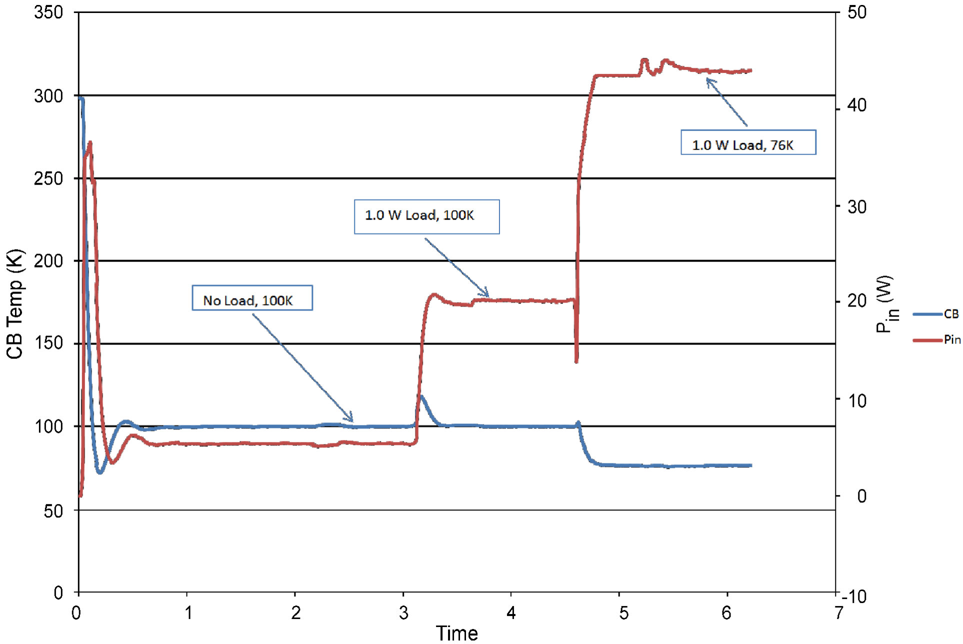


**Figure 7.** Automated cool down on the uPTC and response to load and setpoint transients.

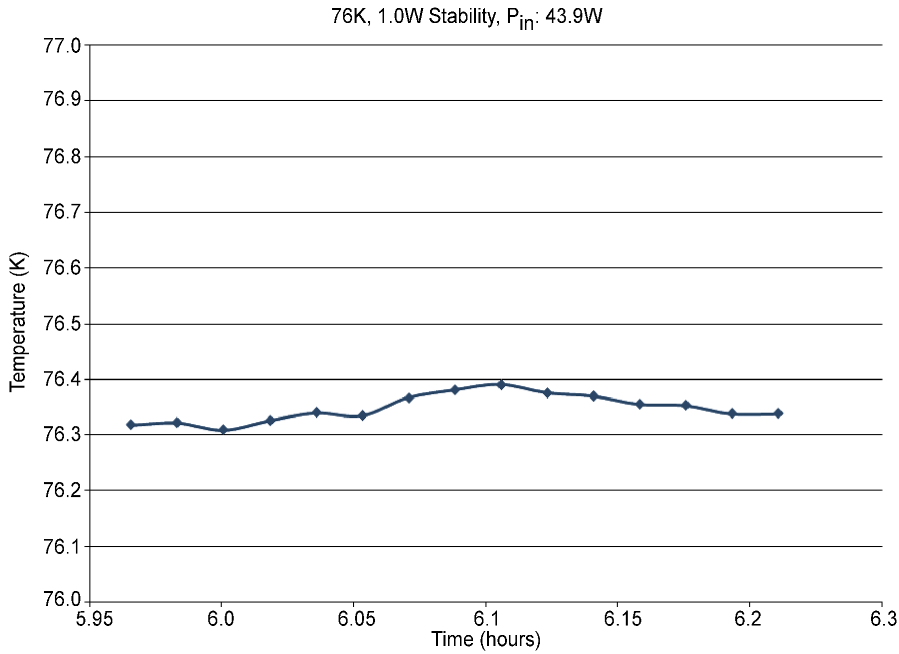


**Figure 8.** Temperature stability at cold-tip with 76K setpoint, 1W thermal load.

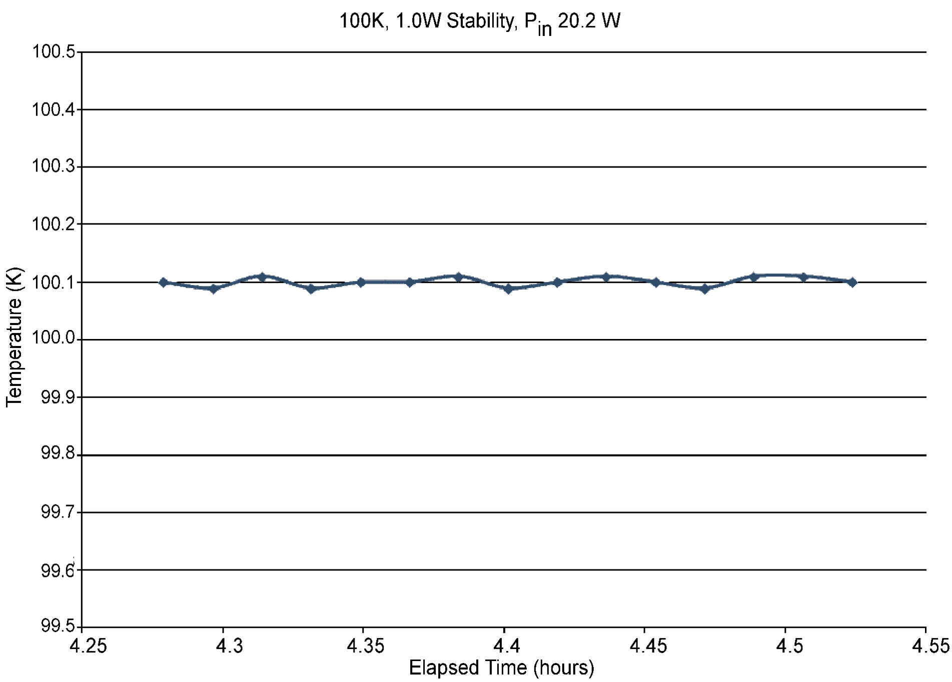


**Figure 9.** Temperature stability at cold-tip with 100K setpoint, 1W thermal load.

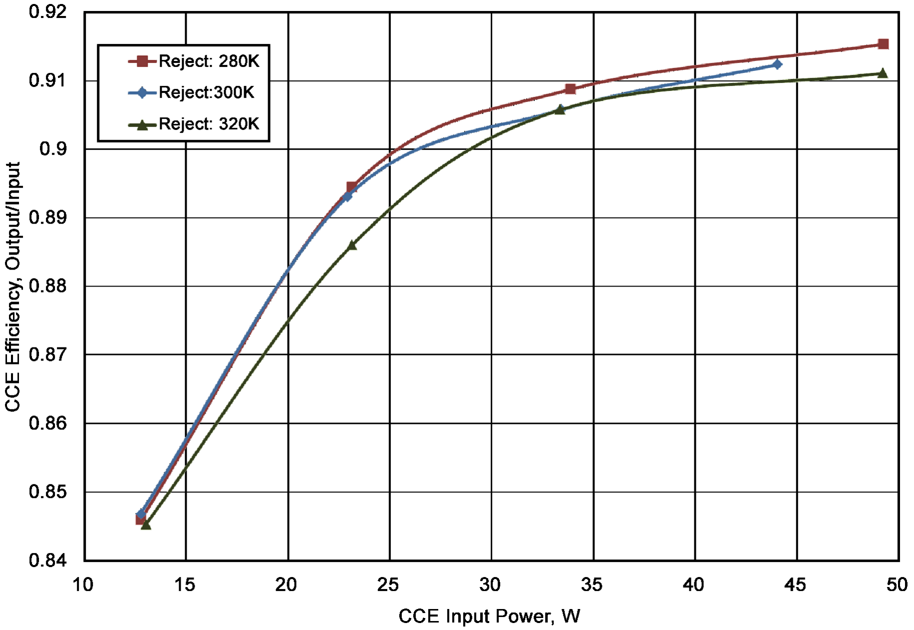


**Figure 10.** LCCE motor drive efficiency as measured while driving the NG Micro PTC.

## ACKNOWLEDGEMENTS

Iris Technology Corporation would like to thank Mr. Jeff Raab and Dr. Emmanuel Tward at Northrop Grumman Aerospace Systems for supporting the testing of the LCCE with the NG Micro PTC at their Redondo Beach facility, and Tanh Nguyen and Glen Toma for their efforts in instrumentation and data collection. Finally, we wish to acknowledge the US Air Force Program Manager, Ms. Erin Pettyjohn, a consistent supporter of our efforts, and without whose foresight this program would not have even happened.

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